CLAIMS

I Claim:

1. A method to dynamically compensate for skew across a plurality of parallel data channels sharing a common clock channel by performing a cold training sequence, comprising the steps of:

   a. sending a training sequence from a source to a receiver across the parallel data channels, the training sequence having a link-reset signature, fence pattern, and source synchronous marker (SSM) byte;

   b. detecting the link-reset signature for a minimum specified amount of time to assure detection in all data channels;

   c. performing delay path calibration for the clock channel;

   d. performing link skew compensation; and

   e. in accordance with the fence pattern, providing word alignment using the SSM byte of the training sequence.

2. The method of claim 1 wherein the plurality of parallel data channels is scalable.

3. The method of claim 1 wherein the link-reset signature is produced by stopping the link clock switching by holding the link clock signal at either a logical one or logical zero state.

4. The method of claim 1 wherein performing link skew compensation consists of a warm training sequence comprising the steps of:

a. sending a second training sequence having a command sub-sequence, second fence pattern, and second SSM byte; and

b. in accordance with the second fence pattern, providing word alignment using the second SSM byte.

5. The method of claim 1, further comprising the steps of:

detecting a system power-up or reset or unrecoverable link error; and

initiating the cold training sequence without the capability to correctly sample or frame an input data stream after system power-up or reset or unrecoverable link error.

6. The method of claim 1, further comprising the steps of:

a. causing a link reset such that the data channels are reset and all calibration values obtained during a previous training sequence are cleared; and

b. immediately initiating a second training sequence.

7. A method to dynamically compensate for skew across a plurality of parallel data channels sharing a common clock channel by performing a warn training sequence, comprising the steps of:

a. sending a training sequence having a command sequence, fence pattern, and source synchronous marker (SSM) byte;

b. in accordance with the fence pattern, providing word alignment using the SSM byte of the training sequence; and

c. in accordance with the command sequence, sending multiple command bytes;

thereby reducing the probability of false or split training sequences due to multiple bit errors.

8. A method to perform dynamic skew compensation across a plurality of parallel data channels sharing a common clock channel without interruption of the clock channel signal and preventing loss of data, comprising the steps of:

a. measuring the clock period of the clock channel signal;

b. determining a clock offset value to properly sample received data from each data channel;

c. performing phase correction of all data channels to the common clock channel by aligning any data edge to any clock edge;

d. identifying data bit zero phase alignment; and

e. adjusting a write location to maintain proper bit ordering.

9. A system to deskew a parallel data link having a plurality of channels for exchanging digital data, the link comprising:

source and destination nodes with an interconnect medium there between;

a Source Synchronous Driver (SSD) at the link source node to format "M" bits of input data received from core logic and to drive "M" data channels onto the link along with a link clock;

a Dynamic Skew Compensation (DSC) architectural block at the link destination node to receive the "M" data bits and link clock and to compensate for skew, recenter the link clock edge relative to the bits of data, and output "M" bits of data, the DSC block comprising:

a DSC bunldle consisting of a plurality of DCS Modules interconnected with a Bundle Interface Module, wherein the DSC Modules perform adjustments to compensate for channel-to-channel skew and substantially center the link clock edge with respect to the data bits.

10. The system of claim 9 wherein the digital data bits are exchanged as pulses of electrical energy over electrically conductive material.

11. The system of claim 9 wherein the digital data bits are exchanged as pulses of light over optic fiber.

12. The system of claim 9 wherein each DSC Module comprises a plurality of DSC Data Channels and a DSC Clock Channel.

13. The system of claim 12 wherein the DSC Clock channel comprises a Clock Channel Front-End block, Built-In Self-Test Logic, and a utility block.

14. The system of claim 13 wherein the Clock Channel Front-End block comprises a finite state machine, Clock Image Latch, Image Decode Logic, String-to-

Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic.

15. The system of claim 12 wherein each DSC Data Channel comprises a Data Channel Front-End block, Data FIFO, and utility block..

16. The system of claim 15 wherein the Data Channel Front-End block comprises a finite state machine, Data Image Latch, Image Decode Logic, String-to-Binary Encoder circuit, DNA logic block, Delay Line, Trim Delay Circuit, and glue logic.

17. The system of claim 15 wherein the Data FIFO comprises a Pattern Search finite state machine, Data FIFO Register File, FIFO Address Encoder, Write Pointer, Read Pointer, Frame Bit Counter, and Skew Synchronizing Marker Start Sequencer.

18. The system of claim 17 wherein the Data FIFO Register File is a write-per-bit FIFO.

19. The system of claim 12 wherein the DSC bundle performs a cold training sequence.

20. The system of claim 12 wherein the DSC bundle performs a warm training sequence.